Amendments to the specification

Please replace the full paragraph commencing at line 5 of page 5 with the following revised paragraph:

The invention also relates to a macro for use as a field programmable gate array embedded in a semiconductor chip. The macro is composed of a plurality of slices, each of which has a unique porosity factor corresponding to the number of wiring channels in the slice. The slices are composed of a plurality of functional blocks. The slices are positioned at locations within the macro wherein the porosity of each slice corresponds to the number of ~~circuits~~ circuit lines in the chip that are intended to pass through wiring channels at each location of the macro. Each of the slices is pre-wired before assembly into the macro. The mass of the blocks with identical functionality is the same. The width and height of the blocks are regular enough to create a normal grid of potential porosity within each slice corresponding to the number of channels across each slice.

Please replace the full paragraph commencing at line 5 on page 11 with the following revised paragraph:

Figure 5 shows a procedure for adjusting the porosity factor according to the teachings of the present invention. The chip array is shown in ~~dotted~~ outline 550. A physical representation 552 of the array with PF marker layers is converted to an LEF (layout exchange format) abstract 554, or other industry accepted or proprietary floor planning abstract format, which contains the porosity factor marker layers that are in the physical representation. The output then goes to the Floorplanning PF Stretch box 560 where input from a PF Adjust Limit Table 558 is used to determine the limits on the degree or amount of stretching that is permissible. One output 570 from box 560 goes to a PF Adjusted T

able 562, the output of which goes to the GDS (graphic design system) merge tool 566 which contains a physical representation of the chip. This merge tool looks at the adjust limits from table 558 and creates the adjusted table 562 telling how much porosity to ~~inset~~ insert into each of the slices. Wires can either be drawn longer or can be augmented with spacer kernels. The spacer GDS kernels 564 are identified with an asterisk to show that their placement is an option to wire stretching. If the spacer kernels are used, they are then inserted into the plan at 566 where required to produce the final chip layout at 568.